IN THE CLAIMS

Amend Claim 42 so that the claims are as follows:

1. (Canceled)

2. (Previously presented) The ESD protection structure of Claim 8, wherein said first conductivity type is n-type, and said second conductivity type is p-type.

3. (Previously presented) The ESD protection structure of Claim 8, wherein said first conductivity type is p-type, and said second conductivity type is n-type.

4. (Canceled)

5. (Previously presented) The ESD protection structure of Claim 8, wherein said third semiconductor region includes a well region of said first conductivity type formed in a semiconductor substrate of said second conductivity type.

6. (Previously presented) The ESD protection structure of Claim 5, wherein each of said second and fourth semiconductor regions includes a base region of said second conductivity type formed in said well region.

7. (Previously presented) The ESD protection structure of Claim 6, further including a pair of heavily doped semiconductor regions of said second conductivity type, each formed in a different one of said base regions.

8. (Previously presented) An electrostatic discharge (ESD) protection structure for protecting an integrated circuit, said ESD protection structure comprising:

a first semiconductor region of a first conductivity type;

a second semiconductor region of a second conductivity type continuous with said first semiconductor region, said second conductivity type being opposite to said first conductivity type;

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an electrically floating third semiconductor region of said first conductivity type continuous with said second semiconductor region and separated from said first semiconductor region by said second semiconductor region;

a fourth semiconductor region of said second conductivity type continuous with said third semiconductor region and separated from said second semiconductor region by said third semiconductor region;

a fifth semiconductor region of said first conductivity type continuous with said fourth semiconductor region and separated from said third semiconductor region by said fourth semiconductor region;

a first terminal connected to said first and second semiconductor regions;

a second terminal connected to said fourth and fifth semiconductor regions;

a first resistor coupled between said first terminal and said second semiconductor region;

a first current source coupled between said terminals so as to be in series with said first resistor;

a second resistor coupled between said second terminal and said fourth semiconductor region; and

a second current source coupled between said terminals so as to be in series with said second resistor.

9 - 20. (Canceled)

21. (Previously presented) An electrostatic discharge (ESD) protection structure for protecting an integrated circuit, said ESD protection structure, comprising:

a first semiconductor region of a first conductivity type;

a second semiconductor region of a second conductivity type continuous with said first semiconductor region, said second conductivity type being opposite to said first conductivity type;

an electrically floating third semiconductor region of said first conductivity type continuous with said second semiconductor region and separated from said first semiconductor region by said second semiconductor region;

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a fourth semiconductor region of said second conductivity type continuous with said third semiconductor region and separated from said second semiconductor region by said third semiconductor region;

a fifth semiconductor region of said first conductivity type continuous with said fourth semiconductor region and separated from said third semiconductor region by said fourth semiconductor region;

a first terminal connected to said first and second semiconductor regions;

a second terminal connected to said fourth and fifth semiconductor regions;

a first resistor coupled between said first terminal and said second semiconductor region;

a first pair of back-to-back diodes coupled between said terminals so as to be in series with said first resistor;

a second resistor coupled between said second terminal and said fourth semiconductor region; and

a second pair of back-to-back diodes coupled between said terminals so as to be in series with said second resistor.

23 - 25. (Canceled)

22. (Previously presented) The ESD protection structure of Claim 21, wherein said diodes are Zener diodes.

26. (Previously presented) The ESD protection structure of Claim 21, wherein said first conductivity type is n-type, and said second conductivity type is p-type.

27. (Previously presented) The ESD protection structure of Claim 21, wherein said first conductivity type is p-type, and said second conductivity type is n-type.

28. (Previously presented) The ESD protection structure of Claim 21, wherein said third semiconductor region includes a well region of said first conductivity type formed in a semiconductor substrate of said second conductivity type.

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29. (Previously presented) The ESD protection structure of Claim 28, wherein each of said second and fourth semiconductor regions includes a base region of said second conductivity type formed in said well region.

30. (Previously presented) The ESD protection structure of Claim 29, further including a pair of heavily doped semiconductor regions of said second conductivity type, each formed in a different one of said base regions.

31. (Previously presented) The ESD protection structure of Claim 8, wherein said first current source is coupled between said second terminal and said second semiconductor region, and said second current source is coupled between said first terminal and said fourth semiconductor region.

32. (Previously presented) The ESD protection structure of Claim 21, wherein said first pair of Zener diodes are coupled between said second terminal and said second semiconductor region, and said second pair of Zener diodes are coupled between said first terminal and said fourth semiconductor region.

33. (Previously presented) A method comprising:

providing an integrated circuit with an electrostatic discharge (ESD) protection structure comprising (a) a first semiconductor region of a first conductivity type connected to a first terminal, (b) a second semiconductor region of a second conductivity type connected to said first terminal and continuous with said first semiconductor region, said second conductivity type being opposite to said first conductivity type, (c) an electrically floating third semiconductor region of said first conductivity type continuous with said second semiconductor region and separated from said first semiconductor region by said second semiconductor region, (d) a fourth semiconductor region of said second conductivity type connected to a second terminal, continuous with said third semiconductor region, and separated from said second semiconductor region by said third semiconductor region, and (e) a fifth semiconductor region of said first conductivity type connected to said second terminal, continuous with said fourth semiconductor region, and separated from said third semiconductor region by said fourth semiconductor region; and

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subjecting said integrated circuit to a voltage of value greater than a trigger magnitude such that the voltage is placed across said terminals and such that current dissipating the voltage automatically flows through said ESD protection structure when the voltage is placed across said terminals.

34. (Previously presented) The method of Claim 33, wherein said first and second conductivity types respectively are n-type and p-type.

35. (Previously presented) The method of Claim 33, wherein said first and second conductivity types respectively are p-type and n-type.

36. (Previously presented) The method of Claim 33 wherein the providing act includes providing said second and fourth semiconductor regions with more heavily doped portions that respectively contact said first and second terminals.

37. (Previously presented) The method of Claim 36, wherein said more heavily doped portion of said second semiconductor region is spaced apart from said first semiconductor region, and said more heavily doped portion of said fourth semiconductor region is spaced apart from said fifth semiconductor region.

38. (Previously presented) The method of Claim 33, wherein the providing act includes forming said ESD protection structure with (a) a first resistor coupled between said first terminal and said second semiconductor region, (b) a first current source coupled between said terminals so as to be in series with said first resistor, (c) a second resistor coupled between such second terminal and said fourth semiconductor region, and (d) a second current source coupled between said terminals so as to be in series with said second resistor.

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39. (Previously presented) The method of Claim 38, wherein the providing act includes providing said ESD protection structure so that said first current source is coupled between said second terminal and said second semiconductor region and so that said second current source is coupled between said first terminal and said fourth semiconductor region.

40. (Previously presented) The method of Claim 33, wherein the providing act includes forming said ESD protection structure with (a) a first resistor coupled between said first terminal and said second semiconductor region, (b) a first pair of back-to-back diodes coupled between said terminals so as to be in series with said first resistor, (c) a second resistor coupled between such second terminal and said fourth semiconductor region, and (d) a second pair of back-to-back diodes coupled between said terminals so as to be in series with said second resistor.

41. (Previously presented) The method of Claim 40, wherein the providing act includes forming said ESD protection structure so that said first current source is coupled between said second terminal and said second semiconductor region and so that said second current source is coupled between said first terminal and said fourth semiconductor region.

42. (Currently amended) The method of Claim 40 wherein said diodes are Zener diodes.

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